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EXAMINER	
PHAM, TAMMY T	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/664,912	KIM ET AL.	
	Examiner	Art Unit	
	TAMMY PHAM	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/28/11*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,8,9,11,12,15-27,29 and 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,8,9,11,12,15-27,29 and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Claims 2-7, 10, 13, 28, 31-47 have been cancelled. Independent claims 1, 30 have been amended. Claims 1, 8-9, 11-12, 15-27, 29-30 are pending. Claims 1, 8 have been withdrawn. Claims 9, 11-12, 15-27, 29-30 are consider below.

Response to Arguments

2. Applicant's arguments filed 28 January 2011 have been fully considered but they are not persuasive.

103 Rejection

3. **In regards to independent claims 9, 30,** Applicant submits that *"a level shifter is a separate element different from a shift register. (Remarks 11)."* This is not persuasive.

4. This argument is moot in view of the new grounds of rejection. In particular, the newly added claim language is not taught within the reference of Cairns1, but rather in the teachings of Nitta.

5. **In regards to independent claims 9, 30,** Applicant submits that *"Fig. 5 of Cairnsl* merely discloses a pair of MUX and DEMUX used in association with DACs in an effort to reduce the circuit area and the number of transistors. See Cairnsl at paragraph 0015. Caimsl thus does not disclose "a multiplexer part performing a time-division on the digital pixel data for

a plurality of data lines for a first horizontal period using a polarity control signal and an even/odd signal" as recited in claim 9 (Remar*ks 11).*" This is not persuasive.

6. In particular, the newly added claim language is not taught within the reference of Cairns1, but rather in the teachings of Nitta. Hence, this argument is moot since Cairns 1 is not relied upon the teach of the limitation as specified above.

7. **In regards to independent claims 9, 30,** Applicant submits that "the Vcom voltage in the claimed invention is supplied to the output channels for a disable period of the input source output enable signal of the second horizontal period. Different from the Vcom voltage, Figure 5 also shows the reference gamma voltage supplied to the PDAC and NDAC so as to convert the *digital signal to the analog signal... Cairnsl does not show that Vcom voltage is supplied to* output portion between an m phase analog driver 22 and matrix 1 (Remarks 11-12)." This is not persuasive.

8. The claim language fails to explicitly teach that the voltage must be supplied "to output portion between an m phase analog driver 22 and matrix 1," hence this argument is moot; and the prior art of record continues to read upon the broadly claimed claim language.

9. **In regards to independent claims 9, 30,** Applicant submits that "Cairns 1 discloses that DACs 21 receive the reference voltage from common reference voltage bus. However, the reference voltage of Cairns 1 corresponds to the reference gamma voltage in Figure 5 of the present application, which is different from the Vcom voltage of the claimed invention. In other

words, the Vcom voltage is a separate element different from the reference gamma voltage as *discussed above (Remarks 13).*" This is not persuasive.

10. The claim language still remains broad. Even assuming that Applicant's assessments are accurate, they are not persuasive because the claim language as currently stated simply teaches of a common voltage that is used for driving the liquid crystal cell. Given this broad definition in the claim language, the teachings of Cairns1 continues to read upon the claim language as currently stated because the common voltage of Cairns1 is used to drive the liquid crystal cell (Fig. 9).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 9, 11-12, 15-27, 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cairns et al. ("Cairns1") (US Patent Application: 2002/0030653 A1) in view of Cairns et al. ("Cairns2") (US Patent No: 6,268,841 B1), Enami et al (US Patent No: 5,892,493), Morita (US Patent No.: 6,989,810 B2), Nitta et al. (U.S. Patent No.: 6,661,402 B2), and Eto et al. (U.S. Patent No: 6,288,697 B1).

12. **As for independent claim 30,** Cairns1 teaches of a data driving method for a liquid crystal display device (Fig. 1), comprising:

13. performing a time-division (Fig. 5, item 13) on a plurality of digital pixel data (Fig. 5, inputs to circuit) for a first horizontal period;

14. supplying the pixel signal (Fig. 5, signals to circuit) to corresponding output channels (Fig. 5, item 5); and

15. outputting a common voltage Vcom to the corresponding data lines (section [0061]), wherein the common voltage Vcom is the voltage for driving a liquid crystal cell (Fig. 1).

16. Cairns1 fails to teach that the pixel data sequentially being outputted to positive and negative paths by unit of adjacent pixel data using a polarity control signal and an even/odd signal;

17. raising a voltage of the time-divided pixel data directly supplied from the positive and negative paths using a level shifter;

18. converting one digital pixel data of the adjacent digital pixel data inputted to the positive path into a positive pixel signal and converting the other digital pixel data of the adjacent digital pixel data inputted to the negative path into a negative pixel signal;

19. sampling and holding the pixel signals and the negative pixel signals during the previous horizontal period of the first horizontal period;

20. simultaneously outputting the held pixel signals (Fig. 5, signals to circuit) to corresponding data lines (Fig. 5, item 5) for an enable period of an input source output enable signal of a second horizontal period and outputting a voltage to the corresponding data lines for a disable period of the input source output enable signal of the second horizontal period,

21. wherein the sampling the pixel signals is controlled by an ODD/EVEN signal performing a time- division on a horizontal period.

22. Nitta teaches of that the pixel data sequentially being outputted to positive and negative paths by unit of adjacent pixel data (Fig. 2) using a polarity control signal and an even/odd signal (Fig. 2, item 216);

23. raising a voltage of the time-divided pixel data (Fig. 2, items 228, 229) directly supplied from the positive and negative paths (Fig. 2, items 228, 229) using a level shifter (Fig. 2, item 231);

24. converting one digital pixel data of the adjacent digital pixel data inputted to the positive path into a positive pixel signal and converting the other digital pixel data of the adjacent digital pixel data inputted to the negative path into a negative pixel signal (Fig. 2).

25. It would have been obvious to one with ordinary skill in the art at the time the invention was made to incorporate the concept of combining the separate the signals in accordance to their polarity as taught by Nitta with the driving circuitry of Cairns1 and Cairns2 in order to improve the picture quality by providing a more efficient driving method (Nitta, column 1, lines 50-55).

26. Cairns2 teaches of sampling (Fig. 11b, item 47-48) and holding (Fig. 11b, item 49-50) the pixel signals.

27. It would have been obvious to one with ordinary skill in the art at the time the invention was made to combine the output part of Cairns2 with the rest of the components of the data driving apparatus of Cairns1 in order to have fewer converters (Cairns2, column 4, lines 33-35).

28. Enami teaches of simultaneously outputting (Fig. 1, item 38) the held pixel signals to corresponding data lines (Fig. 1, item d1A-dnD) for an enable period of an input source output enable signal (Fig. 1, output from item 36).

29. It would have been obvious to one with ordinary skill in the art at the time the invention was made to include a second multiplexer as taught by Enami with the data driver of Cairns1 and the output part of Cairns2 in order to allow the apparatus to perform multiplex driving in which the data voltage is sequentially applied to a number of data lines in each of the data groups (Enami, column 3, lines 49-51).

30. Morita teaches that the signals are separately being supplied during the first half of the horizontal period (Fig. 8, items t2-t7) and during the second half of the horizontal period (Fig. 8, items t8-t13, column 8, lines 18-28);

31. wherein the signals is controlled by an ODD/EVEN signal performing a time- division on a horizontal period (Fig. 8); and

32. outputting a voltage to the corresponding data lines (Fig. 8) for a disable period of the input source output enable signal (Fig. 8).

33. It would have been obvious to one with ordinary skill in the art at the time the invention was made have the signals be supplied separately as taught by Morita with the data driving apparatus of Cairns1, the output part of Cairns2, and the multiplexer part of Enami. The benefits of separating supplying the signals in the first and second horizontal period, is that it allows for a more simple data structure (Morita, column 3, lines 67-1).

34. Eto teaches of the concept of sampling and holding the pixel signals during the previous horizontal period of the first horizontal period (Fig. 11, column 12, lines 15-35).

35. It would have been obvious to one with ordinary skill in the art at the time the invention was made to incorporate the concept of sampling and holding the previous horizontal period of Eto with the signals of Morita, the data driving apparatus of Cairns1, the output part of Cairns2, and the multiplexer part of Enami. One of the benefits of this combination is that it helps improve the displayed image by helping to restrict the variation of the average data line voltage (Eto, column 8, lines 1-3).

36. **As for independent claim 9,** in addition to the claim limitation of claim 30, Cairns1 teaches of performing a certain function for a plurality of data lines (Fig. 9) for a first horizontal period (Fig. 2);

37. of outputting one signal during the first horizontal period with an enabling signal and outputting a reference voltage during a second horizontal signal with a disable period;

38. of the demultiplexer (Fig. 6, item 14) corresponding to the data lines (Fig. 6); and

39. outputting a common voltage Vcom to the corresponding data lines (section [0061]), wherein the common voltage Vcom is the voltage for driving a liquid crystal cell (Fig. 1).

40. Cairns1 fails to teach of a level shifter part raising a voltage of the data;

41. a discharging part connected between output buffers and the data lines and simultaneously outputting the pixel signals held in the holding part for the first horizontal period to corresponding data lines for an enable period of a source output enable signal and outputting a voltage to the corresponding data lines for a disable period of the source output enable signal;

42. wherein the sampling part and the holding part sample and hold the pixel signals supplied for the next horizontal period through the channel different from that of the pixel signal supplied for the first horizontal period.

43. Cairns1 explicitly teaches of a shift register in another embodiment (Fig. 8).

44. It would have been obvious to one with ordinary skill in the art at the time the invention was made to include the shift register of the other embodiment with Cairns since shift registers ensure that all of the flip flop circuits are able to reset to the "zero" logic state before operation (section [0058]).

45. Cairns2 teaches of a discharging part (Fig. 11b, aspects of circuit in which item is discharging) connected between output buffers (Fig. 11b, item 40) and the data lines (Fig. 11b, item 8 and its interconnections); and

46. that the sampling part (Fig. 11b, item 47-48) and the holding part (Fig. 11b, item 49-50) sample and hold the pixel signals supplied for the next horizontal period (Fig. 10, second pulse of item HSYNC) through the channel different (Fig. 10, item Column M/2 +1) from that of the pixel signal supplied for the first horizontal period (Fig. 10, first pulse of item HSYNC).

47. It would have been obvious to one with ordinary skill in the art at the time the invention was made to combine the output part of Cairns2 with the rest of the components of the data driving apparatus of Cairns1 in order to have fewer converters (Cairns2, column 4, lines 33-35).

48. Enami teaches of a discharging part (Fig. 1, item 38) simultaneously outputting the pixel signals held in the holding part for the period to corresponding data lines for an enable period of a source output enable signal (Fig. 1, outputs of item 40) of a second period and outputting a voltage (Fig. 1, outputs of item 38) to the corresponding data lines (Fig. 1, items d1A-dnD).

49. It would have been obvious to one with ordinary skill in the art at the time the invention was made to include a discharging part as taught by Enami with the data driver of Cairns1 and the output part of Cairns2. The benefit of this combination is to allow the apparatus to perform multiplex driving in which the data voltage is sequentially applied to a number of data lines in each of the data groups (Enami, column 3, lines 49-51).

50. **As for claim 11,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the multiplexer part (Cairns1, Fig. 4, item 13) comprises:

51. a plurality of positive path switches coupled to input channels for the pixel data and commonly connected to the positive polarity output channel; and

52. a plurality of negative path switches coupled to the input channels for the pixel data, connected to the positive path switches in parallel, and commonly connected to negative polarity output channel (Cairns1, Fig.4, section [0015]) (Nitta, Fig. 2, column 3, lines 23-33; column 4, lines 35-30).

53. **As for claim 12,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the demultiplexer (Cairns1, Fig. 4, item 14) part comprises: a plurality of positive path switches forming a plurality of different positive paths corresponding to the data lines, and commonly connected to a positive digital-analog converter, and a plurality of negative path switches forming a plurality of different negative paths, commonly connected to a negative digital-analog converter (Id.), wherein the negative path switches are connected to the positive path switches in parallel (Cairns1, Fig.4, section [0015]) (Nitta, Fig. 1, column 3, lines 23-33; column 4, lines 35-30).

54. **As for claim 15,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the sampling part (Cairns2, Fig. 11b) has a second demultiplexer (Cairns2, Fig. 3, item 25) part comprising; a plurality of the positive path switches forming a plurality of different positive paths and connected to the output channels of the demultiplexer part (Id.); and a plurality of negative path switches forming a plurality of different negative paths and connected to the output

channels of the demultiplexer part (Id.) (Cairns2, Fig. 12, column 10, lines 18-41) (Nitta, Fig. 2, column 3, lines 23-33; column 4, lines 35-30).

55. **As for claim 16,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the holding part comprises:

56. positive path capacitors charging and holding the positive pixel signals from the positive path switches of the second demultiplexer (Cairns2, Fig. 3, item 25) part; and

57. negative path capacitors charging and holding the negative pixel signals from the negative path switches of the second demultiplexer (Id.) part in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

58. **As for claim 17,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the discharging part comprises:

59. a second multiplexer part (Cairns1, Fig. 4, item 14) having:

60. a plurality of positive path switches connected to the positive path switches of the second demultiplexer (Cairns1, Fig. 4, item 14) through the holding part and connected to the data lines; and

61. a plurality of negative path switches connected to the negative switches of the second demultiplexer (Id.) through the holding part and connected to the data lines (column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}).

62. **As for claim 18,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the multiplexer, the demultiplexer (Cairns2, Fig. 3, item 25), and the second demultiplexer (Id.) are controlled by a first control signal through an input polarity control signal and an ODD/EVEN signal performing the time-division on a horizontal period in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

63. **As for claim 19,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the ODD/EVEN signal performsthe time-division on an enable period determined by a source output enable signal for the horizontal period in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

64. **As for claim 20,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the ODD/EVEN signal further performs the time-division on a disable period of the source output enable signal in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

65. **As for claim 21,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the multiplexer part, the demultiplexer (14) part in Fig.4 and section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}. The combination of Cairns2 and Nitta teaches that the second demultiplexer (64) part recharge the holding part with the pixel signals for the disable period, wherein the pixel signals are generated for a previous enable

period in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

66. **As for claim 22,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the source output enable signal is generated by increasing the disable period of an external reference source output enable signal in order to secure a recharging period of the holding part in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

67. **As for claim 23,** Cairns1 as modified by Cairns2, Enami and Nitta teaches the second multiplexer part is controlled by the first control signal and a second control signal that is phase-inversed with respect to the first control signal in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

68. **As for claim 24,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that an output buffer (Cairns2, Fig. 11b, item 40) part buffering the pixel signals discharged from the holding part to the discharging part in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

69. **As for claim 25,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the output buffer (Cairns2, Fig. 11b, item 40) part comprises: a plurality of positive path output buffers (Id.) connected between the positive path capacitors of the holding part and the positive path switches

of the second multiplexer part; and a plurality of negative path output buffers (Id.) connected between the negative path capacitors of the holding part and the negative path switches of the second multiplexer part in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

70. **As for claim 26,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the output buffer (Cairns2, Fig. 11b, item 40) part buffering the pixel signal supplied through the output channels of the second multiplexer part and supplying the pixel signals to each of the data lines in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

71. **As for claim 27,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the output buffer (Cairns2, Fig. 11b, item 40) part comprises: a plurality of output buffers (Cairns2, Fig. 11b, item 40) connected between the output channels of the second multiplexer part and the data lines in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

72. **As for claim 29,** Cairns1 as modified by Cairns2, Enami and Nitta teaches of: teaches that a third multiplexer part supplying the pixel signals from the output part to the corresponding data lines for the enable period of the source output enable signal and commonly supplying a reference voltage of the liquid crystal cells to the corresponding data lines for the disable period

of the source output enable signal in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

Conclusion

73. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

74. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

75. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tammy Pham whose telephone number is (571) 272-7773. The examiner can normally be reached on 8:00-5:30 (Mon-Fri).

76. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

77. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TP

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/Tammy Pham/
Examiner, Art Unit 2629